

WHAT IS CLAIMED IS:

1 1. A charge pump comprising:

2 a first current mirror capable of injecting a first
3 charging current, $I(U)$, onto a loop filter coupled to an output
4 of said charge pump and injecting a second charging current,
5 $I(U)/M$, onto an integrator capacitor, wherein said first and
6 second charging currents are controlled by a first common control
7 signal such that said first charging current mirrors said second
8 charging current by a factor M ;

9 a second current mirror capable of draining a first
10 discharging current, $I(D)$, from said loop filter and draining a
11 second discharging current, $I(D)/M$, from said integrator
12 capacitor, wherein said first and second discharging currents are
13 controlled by a second common control signal such that said first
14 discharging current mirrors said second discharging current by
15 said factor M ;

16 a sampling circuit capable of coupling said second
17 charging current and said second discharging current to said
18 integrator capacitor so that said integrator capacitor is one of:
19 i) charged and ii) discharged by a difference current between
20 said second charging current and said second discharging current;
21 and

22 a control circuit capable of detecting a voltage

23 difference between a voltage on said loop filter and a voltage on
24 said integrator capacitor, wherein said control circuit is
25 operable to adjust said first common control signal to minimize
26 said voltage difference.

1 2. The charge pump as set forth in Claim 1 wherein said
2 first current mirror comprises:

3 a first charging current source capable of injecting
4 said first charging current onto said loop filter; and

5 a second charging current source capable of injecting
6 said second charging current onto said integrator capacitor.

1 3. The charge pump as set forth in Claim 2 wherein said
2 second current mirror comprises:

3 a first discharging current source capable of draining
4 said first discharging current from said loop filter; and

5 a second discharging current source capable of draining
6 said second discharging current from said integrator capacitor.

1 4. The charge pump as set forth in Claim 1 wherein said
2 control circuit comprises an amplifier having a non-inverting
3 input coupled to said integrator capacitor and an inverting input
4 coupled to said loop filter.

1 5. The charge pump as set forth in Claim 4 wherein said
2 first common control voltage is generated on an output of said
3 amplifier.

1 6. The charge pump as set forth in Claim 1 wherein said
2 control circuit, in response to an increase in voltage on said
3 integrator capacitor, adjusts said first common control voltage
4 so that said second charging current is reduced.

1 7. The charge pump as set forth in Claim 6 wherein said
2 adjustment of said first common control voltage by said control
3 circuit also reduces said first charging current.

1 8. The charge pump as set forth in Claim 1 wherein said
2 control circuit, in response to a decrease in voltage on said
3 integrator capacitor, adjusts said first common control voltage
4 so that said second charging current is increased.

1 9. The charge pump as set forth in Claim 8 wherein said
2 adjustment of said first common control voltage by said control
3 circuit also increases said first charging current.

1 10. An integrated circuit comprising:
2 a system control section capable of operating at a
3 plurality of clock speeds;
4 at least one of a phase-locked loop (PLL) and a delay-
5 locked loop (DLL) capable of providing at least one clock signal
6 to said system control section, said at least one of a PLL and a
7 DLL comprising a charge pump, wherein said charge pump comprises:
8 a first current mirror capable of injecting a
9 first charging current, $I(U)$, onto a loop filter coupled to
10 an output of said charge pump and injecting a second
11 charging current, $I(U)/M$, onto an integrator capacitor,
12 wherein said first and second charging currents are
13 controlled by a first common control signal such that said
14 first charging current mirrors said second charging current
15 by a factor M ;
16 a second current mirror capable of draining a
17 first discharging current, $I(D)$, from said loop filter and
18 draining a second discharging current, $I(D)/M$, from said
19 integrator capacitor, wherein said first and second
20 discharging currents are controlled by a second common
21 control signal such that said first discharging current
22 mirrors said second discharging current by said factor M ;
23 a sampling circuit capable of coupling said

24 second charging current and said second discharging current
25 to said integrator capacitor so that said integrator
26 capacitor is one of: i) charged and ii) discharged by a
27 difference current between said second charging current and
28 said second discharging current; and

29 a control circuit capable of detecting a voltage
30 difference between a voltage on said loop filter and a
31 voltage on said integrator capacitor, wherein said control
32 circuit is operable to adjust said first common control
33 signal to minimize said voltage difference.

1 11. The integrated circuit as set forth in Claim 10 wherein
2 said first current mirror comprises:

3 a first charging current source capable of injecting
4 said first charging current onto said loop filter; and

5 a second charging current source capable of injecting
6 said second charging current onto said integrator capacitor.

1 12. The integrated circuit as set forth in Claim 11 wherein
2 said second current mirror comprises:

3 a first discharging current source capable of draining
4 said first discharging current from said loop filter; and

5 a second discharging current source capable of draining
6 said second discharging current from said integrator capacitor.

1 13. The integrated circuit as set forth in Claim 10 wherein
2 said control circuit comprises an amplifier having a non-
3 inverting input coupled to said integrator capacitor and an
4 inverting input coupled to said loop filter.

1 14. The integrated circuit as set forth in Claim 13 wherein
2 said first common control voltage is generated on an output of
3 said amplifier.

1 15. The integrated circuit as set forth in Claim 10 wherein
2 said control circuit, in response to an increase in voltage on
3 said integrator capacitor, adjusts said first common control
4 voltage so that said second charging current is reduced.

1 16. The integrated circuit as set forth in Claim 15 wherein
2 said adjustment of said first common control voltage by said
3 control circuit also reduces said first charging current.

1 17. The integrated circuit as set forth in Claim 10 wherein
2 said control circuit, in response to a decrease in voltage on
3 said integrator capacitor, adjusts said first common control
4 voltage so that said second charging current is increased.

1 18. The integrated circuit as set forth in Claim 17 wherein
2 said adjustment of said first common control voltage by said
3 control circuit also increases said first charging current.

1 19. A method of operating a charge pump, the charge pump
2 comprising: 1) a first current mirror capable of injecting a
3 first charging current onto a loop filter coupled to an output of
4 the charge pump and injecting a second charging current onto an
5 integrator capacitor, wherein the first and second charging
6 currents are controlled by a first common control signal such
7 that the first charging current mirrors the second charging
8 current by a factor M; 2) a second current mirror capable of
9 draining a first discharging current from the loop filter and
10 draining a second discharging current from the integrator
11 capacitor, wherein the first and second discharging currents are
12 controlled by a second common control signal such that the first
13 discharging current mirrors the second discharging current by the
14 factor M, wherein the method comprises the steps of:

15 coupling the second charging current and the second
16 discharging current to the integrator capacitor so that the
17 integrator capacitor is one of: i) charged and ii) discharged by
18 a difference current between the second charging current and the
19 second discharging current;

20 detecting a voltage difference between a voltage on the
21 loop filter and a voltage on the integrator capacitor; and

22 in response to the detection of the voltage difference,
23 adjusting the first common control signal to minimize the voltage
24 difference.

1 20. The method as set forth in Claim 19 wherein, in
2 response to an increase in voltage on the integrator capacitor,
3 the step of adjusting adjusts the first common control voltage so
4 that the second charging current is reduced.

1 21. The method as set forth in Claim 20 wherein the step of
2 adjusting also reduces the first charging current.

1 22. The method as set forth in Claim 19 wherein, in
2 response to a decrease in voltage on the integrator capacitor,
3 the step of adjusting adjusts the first common control voltage so
4 that the second charging current is increased.

1 23. The method as set forth in Claim 22 wherein the step of
2 adjusting also increases the first charging current.